

1            **ABSTRACT**

2            A memory architecture includes a first substrate containing multiple  
3            memory devices and a first channel portion extending across the first substrate.  
4            The architecture further includes a second substrate containing multiple memory  
5            devices and a second channel portion extending across the second substrate. A  
6            connector couples the first channel portion to the second channel portion to form a  
7            single channel. The connector includes a first slot that receives an edge of the first  
8            substrate and a second slot that receives an edge of the second substrate. Another  
9            connector has a pair of slots that receive opposite edges of the first and second  
10          substrates. The channel portions extend across the substrates in a substantially  
11          linear path. Each channel portion includes multiple conductors having lengths that  
12          are approximately equal.